Claims

We claim:

1. A memory array comprising a plurality of floating gate transistors connected in series, each floating gate transistor having formed, in a well of a substrate, a source and a drain region and a channel region separating said source and drain regions, said channel region having a non-uniform concentration of dopant.

2. The memory array of claim 1, wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction from the surface of the substrate.

3. The memory array of claim 2, wherein said non-uniform concentration comprises a lateral concentration distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

4. The memory array of claim 1 wherein the non-uniform concentration is formed by a tilted ion implantation utilizing as a mask a gate structure of each floating gate NMOS transistor.

5. A method for making a memory array comprising:

forming a plurality of floating gate NMOS transistors connected in series, each having a source and a drain region and a channel region separating the source and the drain regions, and

implanting beneath a central portion of the channel region a non-uniform concentration of dopant.

6. The method of claim 5, wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction away from the surface of the substrate.

7. The method of claim 6, wherein said non-uniform concentration comprises a lateral distribution along the length of the channel region that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

8. The method of claim 5, wherein said non-uniform concentration is provided by a tilted ion implantation utilizing as a mask a gate structure of each floating gate transistor.

9. An isolated gate floating gate NMOS transistor comprising, in a well structure of a substrate, a source and a drain region and a channel region separating the source and the drain region, said channel region having a non-uniform concentration of dopant.

10. The transistor of claim 9, wherein said non-uniform concentration comprises a retrograde concentration distribution in the direction away from the surface of the substrate.

11. The transistor of claim 10, wherein said non-uniform concentration comprises a lateral concentration

distribution along the length of the channel that is higher in a region generally towards the central portion of the channel region and decreases toward the opposing source and drain regions.

12. The transistor of claim 9 wherein said non-uniform distribution is provided by a tilted ion implantation utilizing as a mask at least part of a gate structure of said transistor.